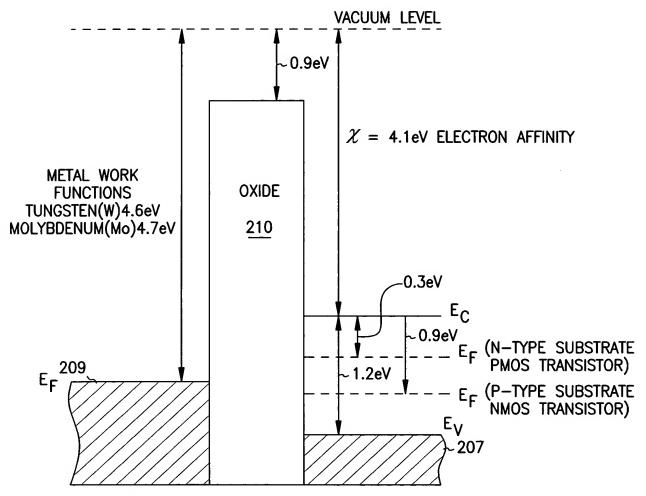


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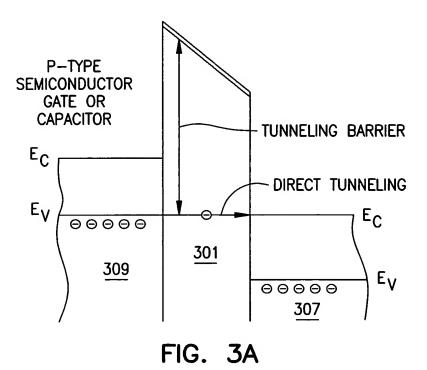
2/7

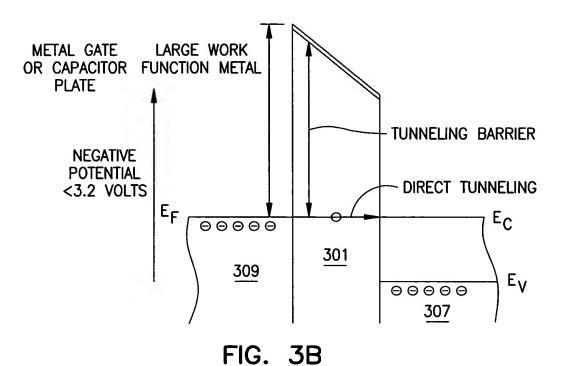


"MID-GAP" METALS USED FOR OPTIMIZING NMOS AND PMOS TRANSISTOR THRESHOLDS VOLTAGES; METAL SEMICONDUCTOR WORK FUNCTION DIFFERENCES

NMOS:  $\overline{\Phi}$ ms = 4.7-5.0eV = -0.3V PMOS:  $\overline{\Phi}$ ms = 4.7-4.4eV = +0.3V

FIG. 2 (PRIOR ART)





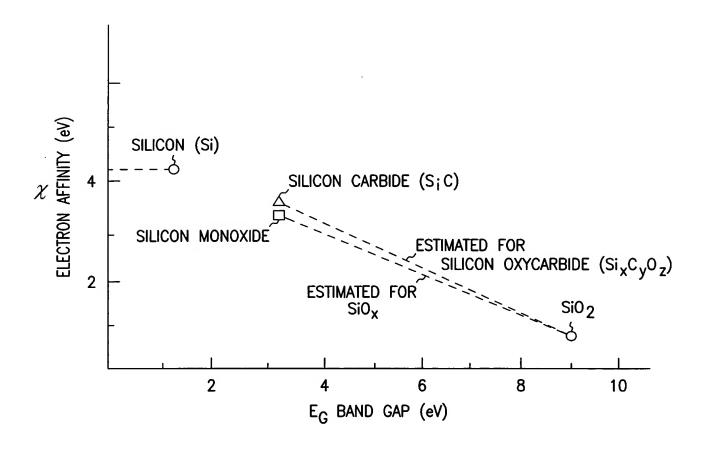


FIG. 4

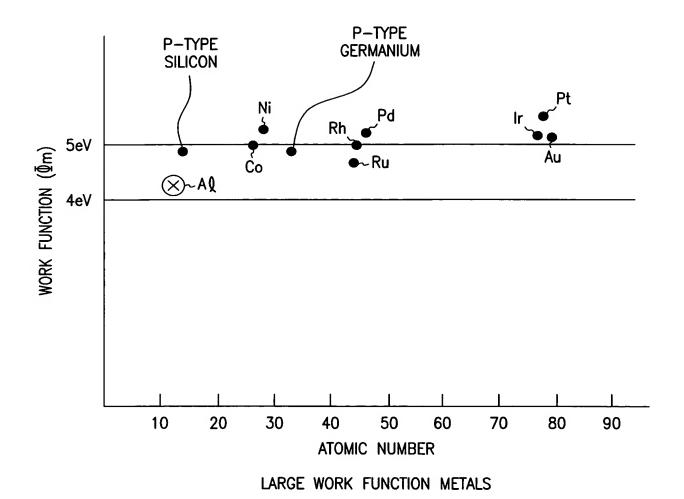


FIG. 5



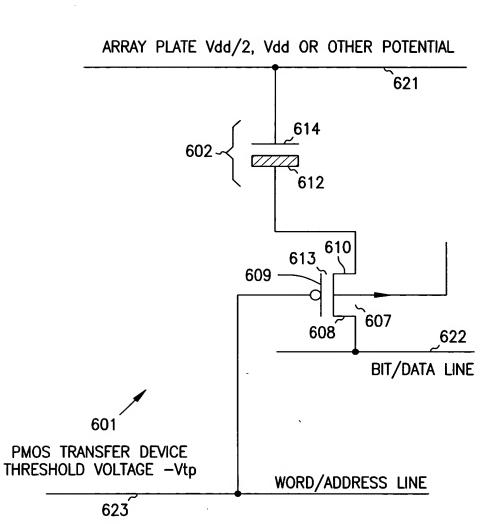


FIG. 6

TITLE: TECHNIQUE TO CONTROL TUNNELING CURRENTS IN DRAM CAPACITORS, CELLS, AND DEVICES INVENTORS NAME: Leonard Forbes et al.

DOCKET NO.: 1303.017US2

